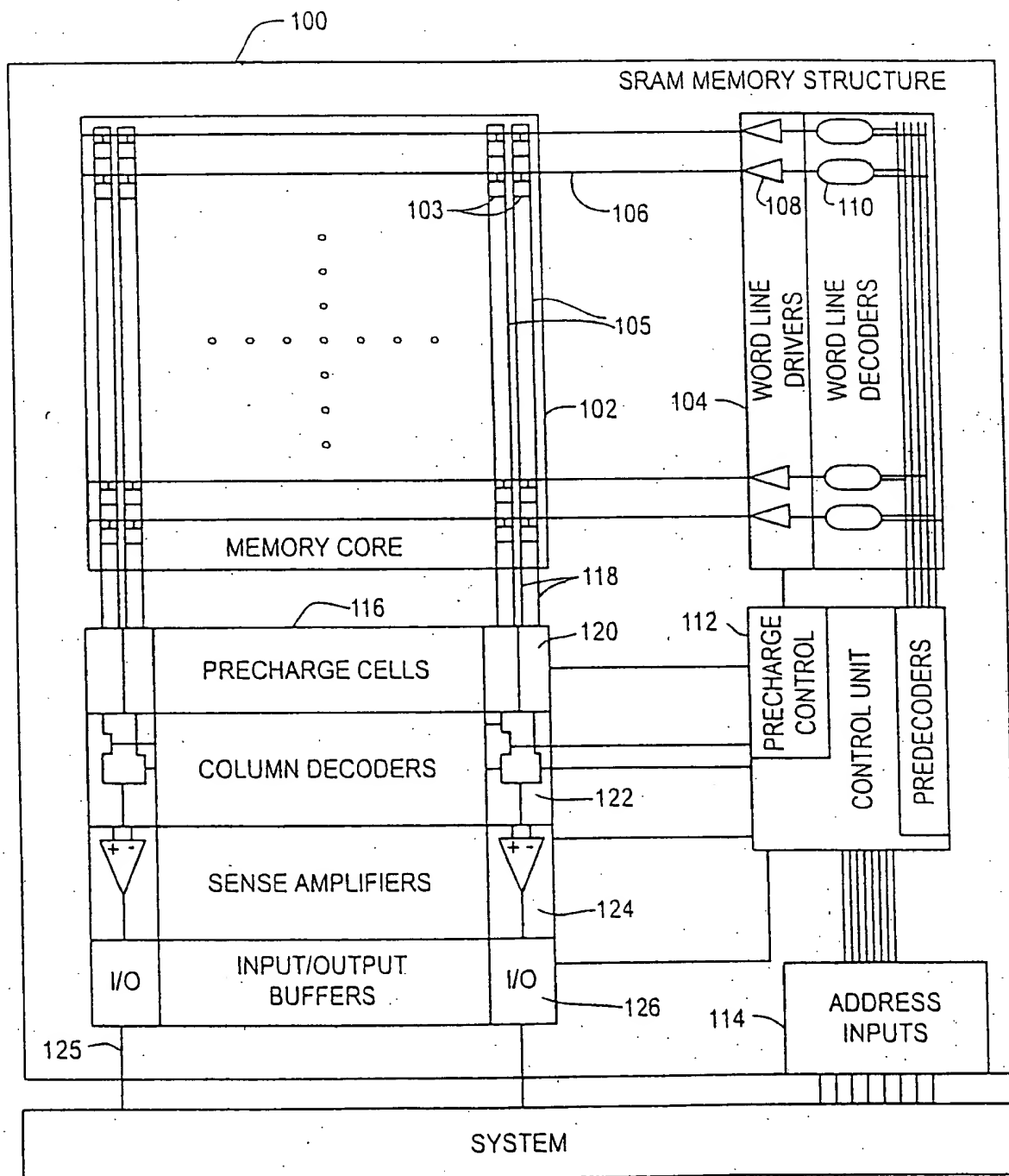




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Fig. 1



PRIOR ART



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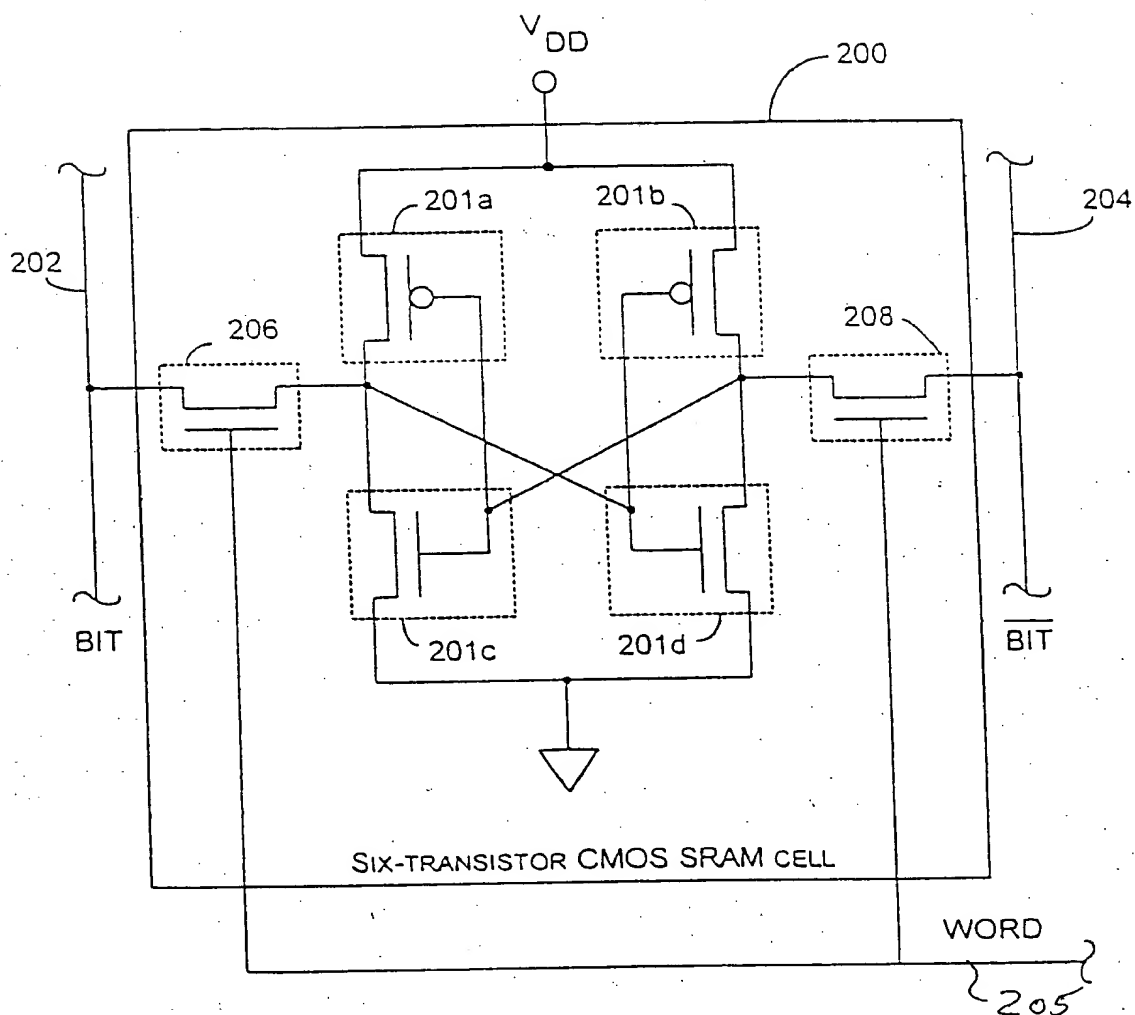


FIG. 2



TITLE: Asynchronously-Resettable Decoder
With Redundancy
INVENTOR: Terzioglu et al.
APPLICATION NO.: 09/775,476,
CONF. NO. 7751; DOCKET NO. 13451US02
ATTORNEY: REL, PHONE: 312-775-8000

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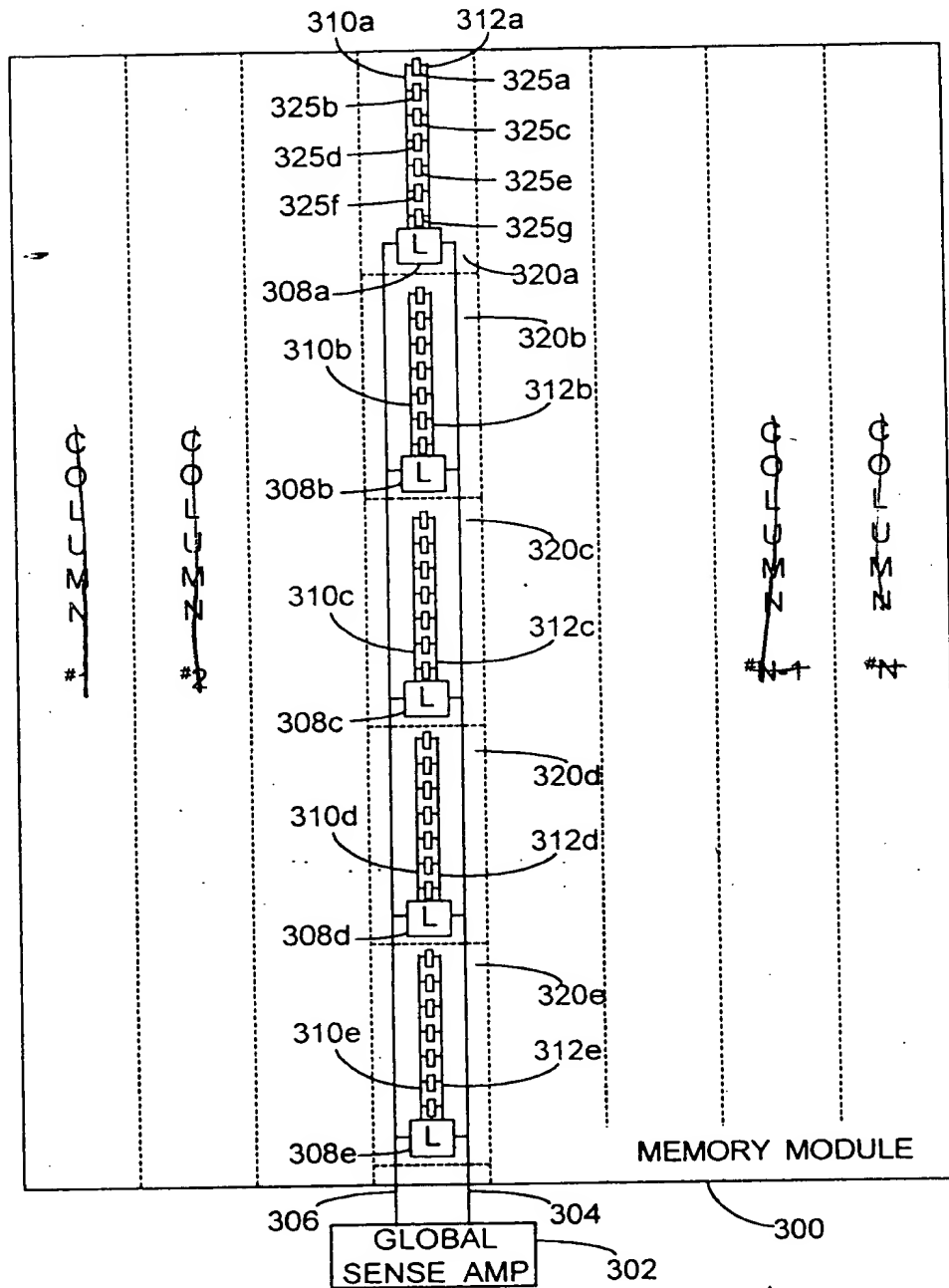
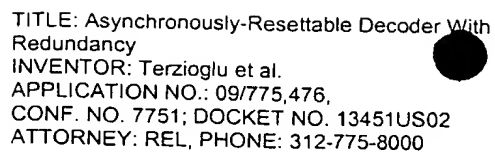


FIG. 3

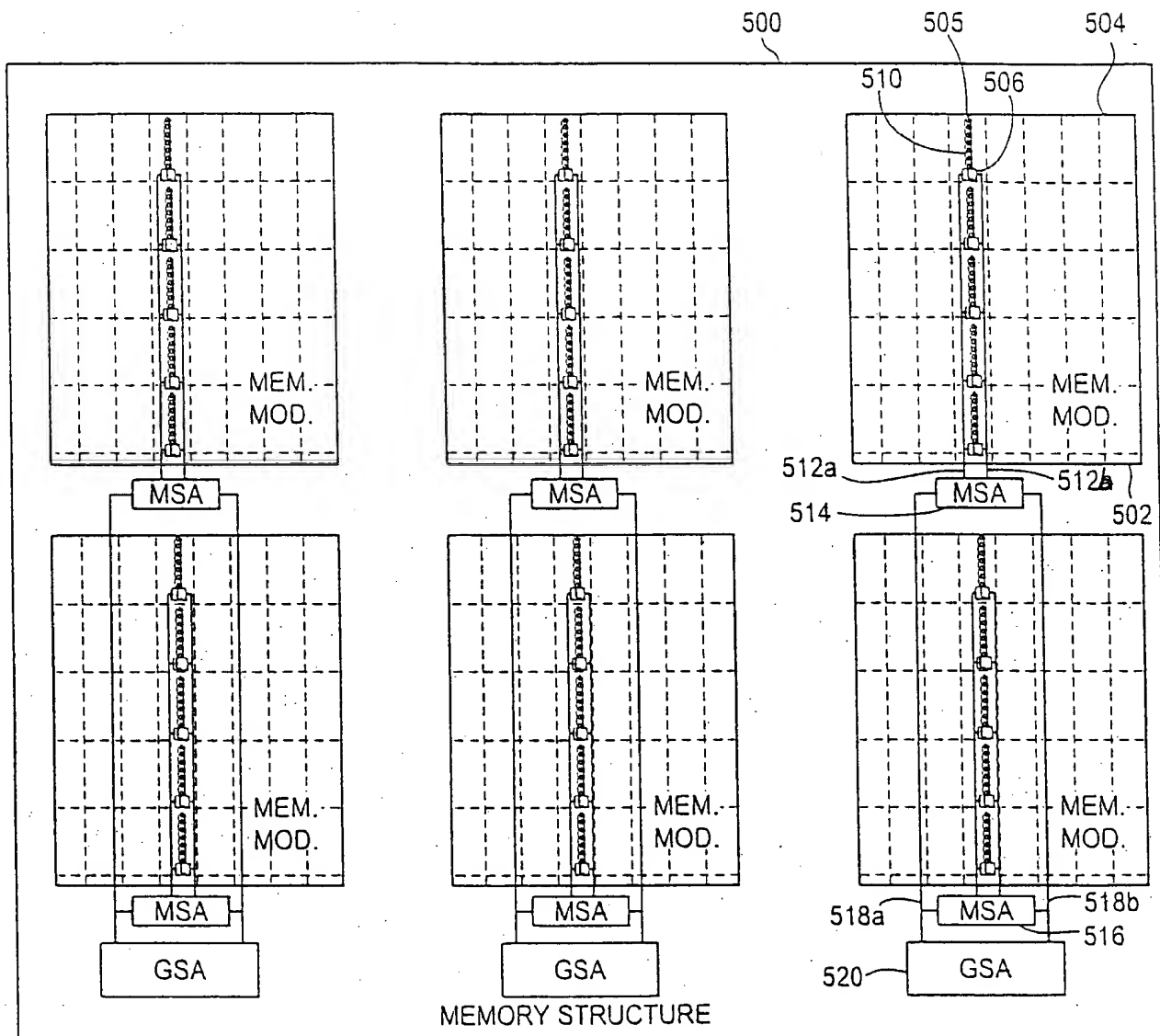


This schematic diagram illustrates a memory array structure. A central vertical column of memory cells is connected to a horizontal bus labeled "GLOBAL SENSE AMP" at the bottom. The array is divided into four vertical sections by dashed lines. The central column is flanked by two columns of memory cells, each containing a series of cells labeled 410a through 410d and 412a through 412d. The central column itself contains a series of cells labeled 420a through 420d and 425a through 425g. The entire structure is labeled "MEMORY BLOCK" and is connected to a "GLOBAL SENSE AMP" at the bottom, which is further connected to a "GLOBAL SENSE AMP" at the bottom right. The diagram is labeled with various reference numerals: 400, 402, 404, 406, 410a, 410b, 410c, 410d, 412a, 412b, 412c, 412d, 420a, 420b, 420c, 420d, 425a, 425b, 425c, 425d, 425e, 425f, 425g, and 408a through 408d.



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FIG. 5



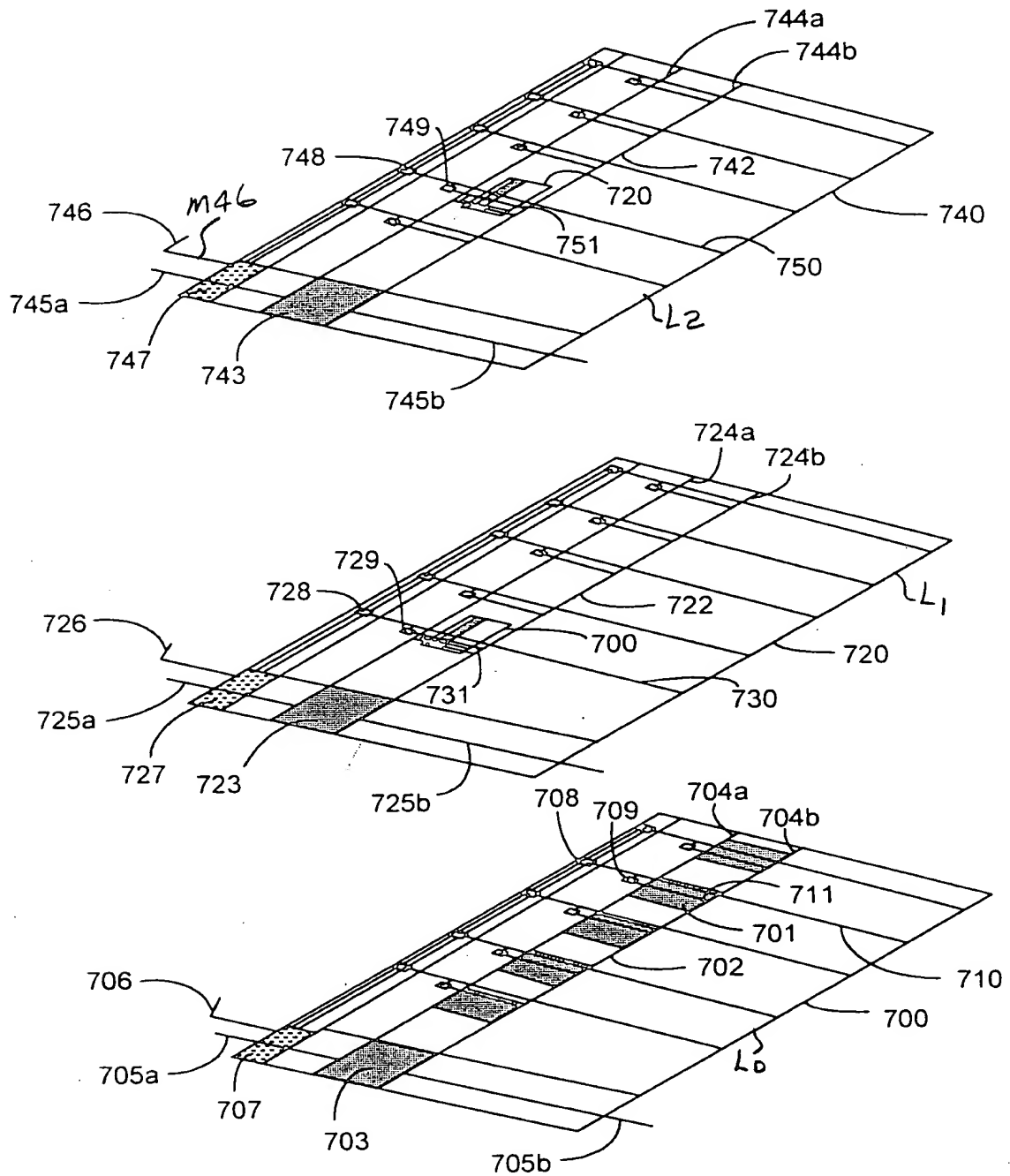


FIG. 7



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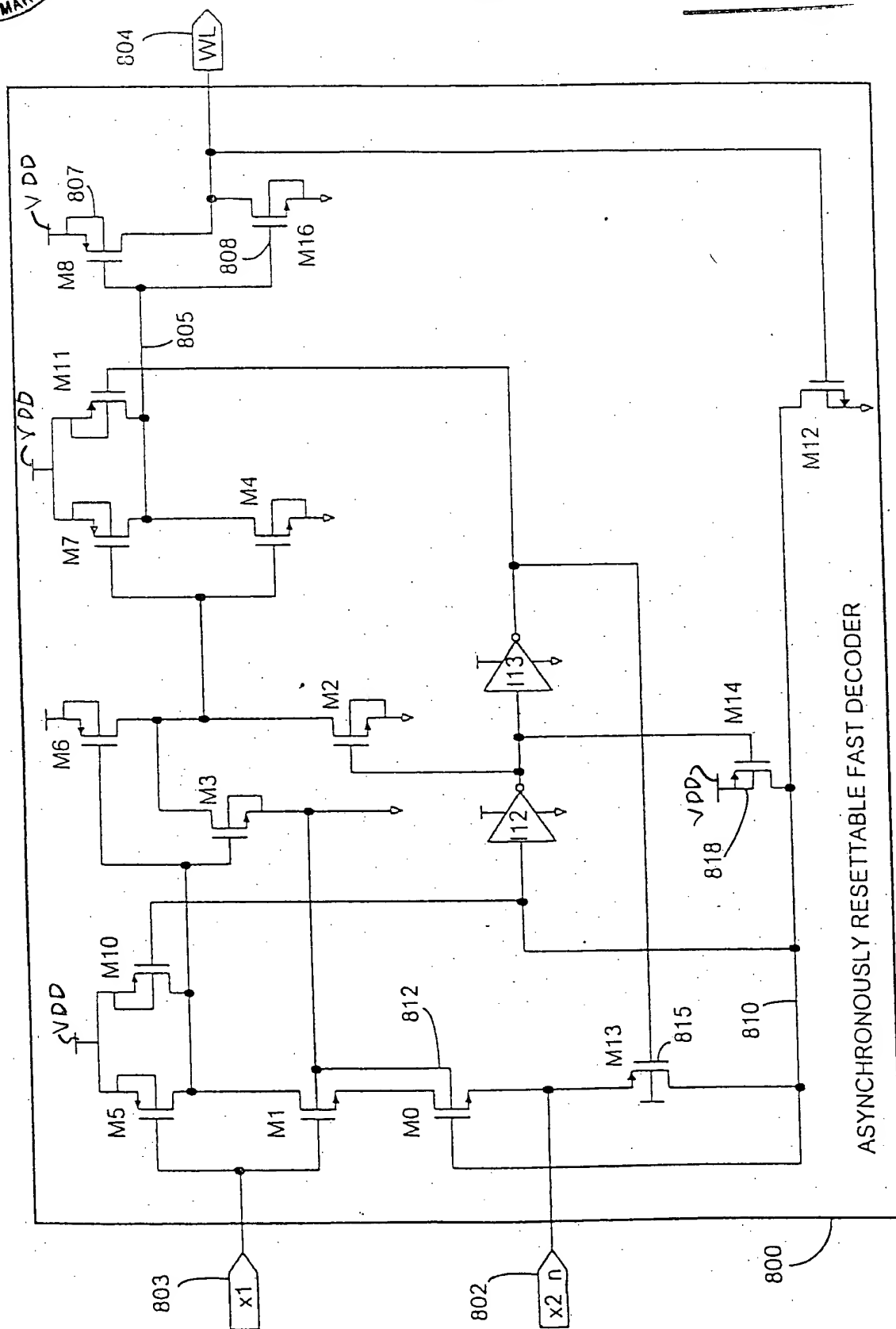
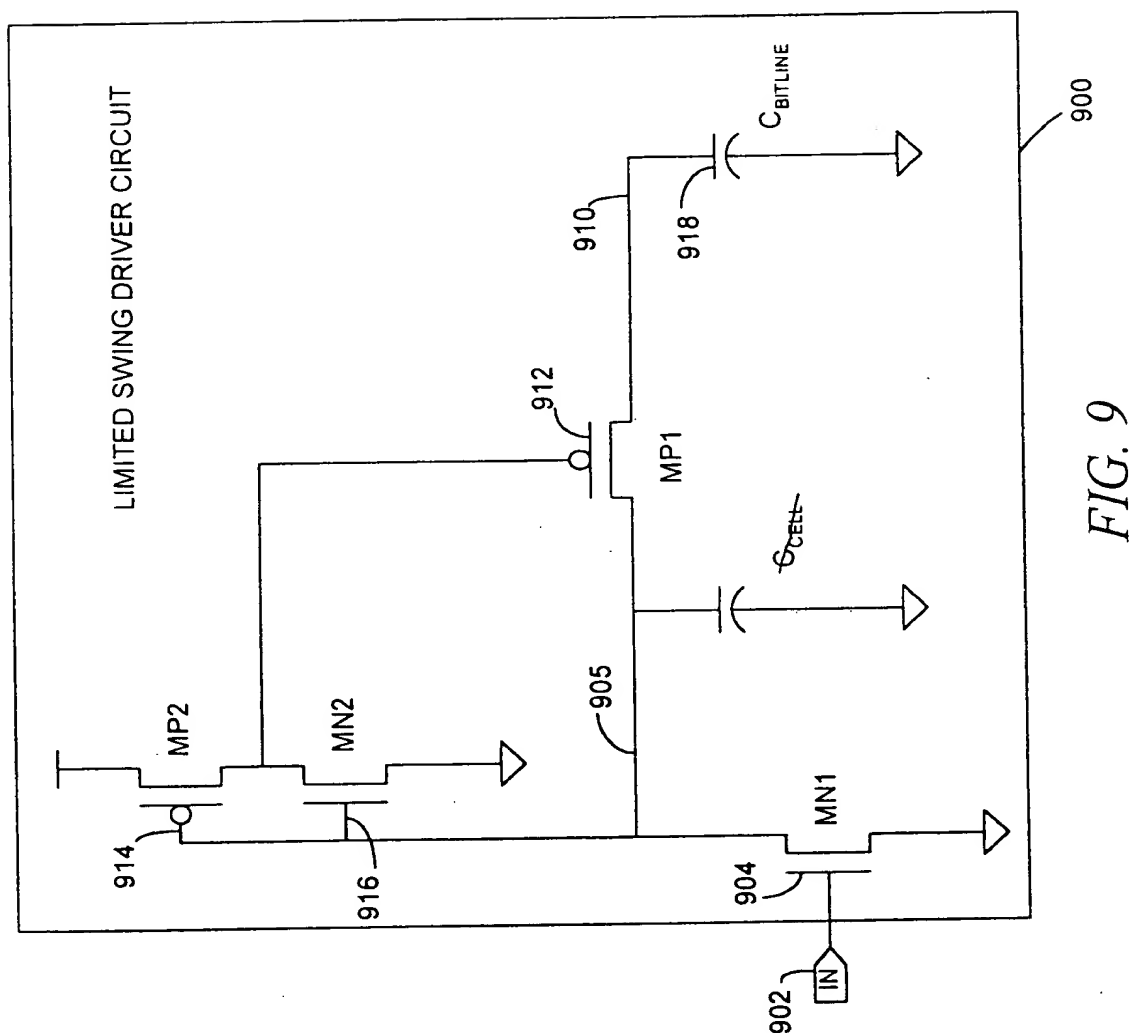


FIG. 8



TITLE: Asynchronously-Resetable Decoder With
Redundancy
INVENTOR: Terzioglu et al.
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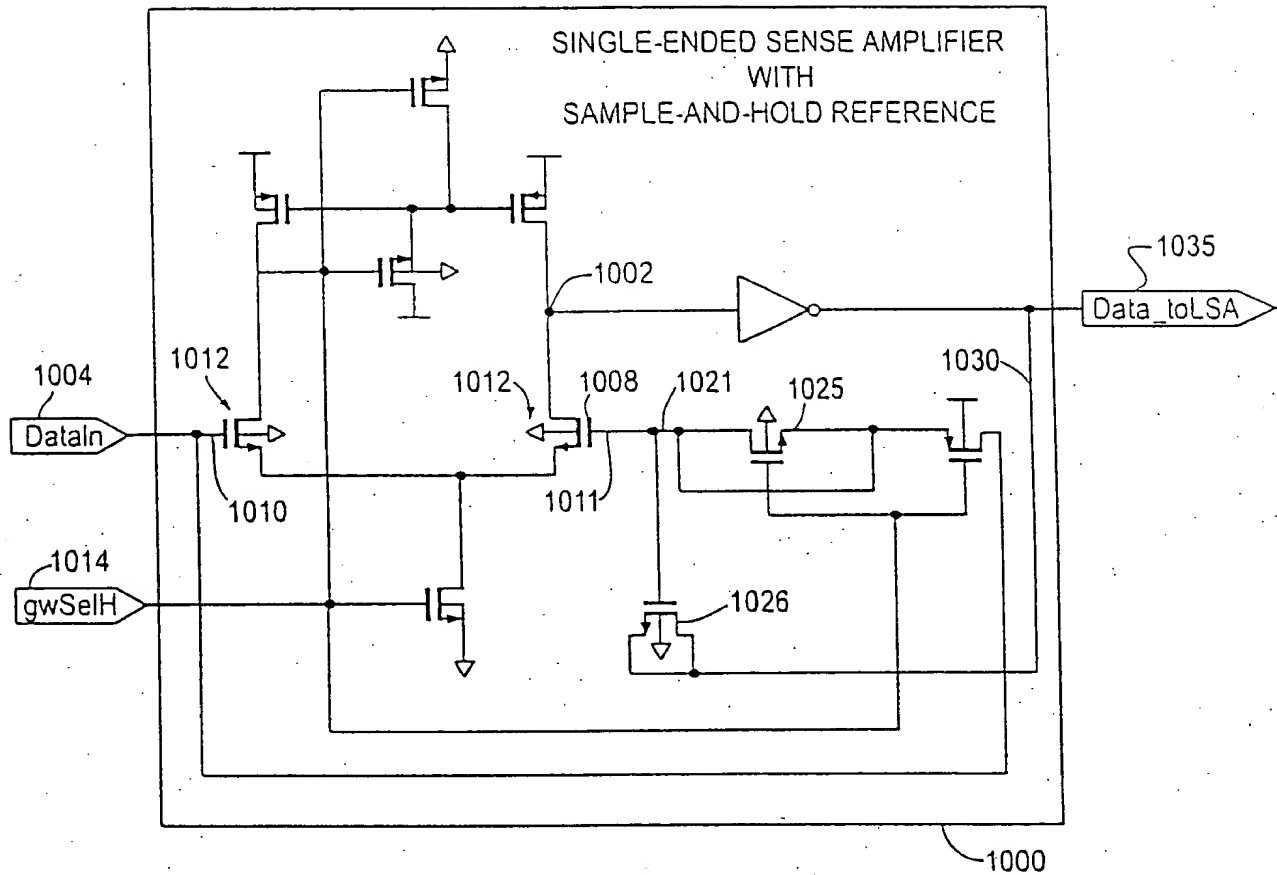
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FIG. 10





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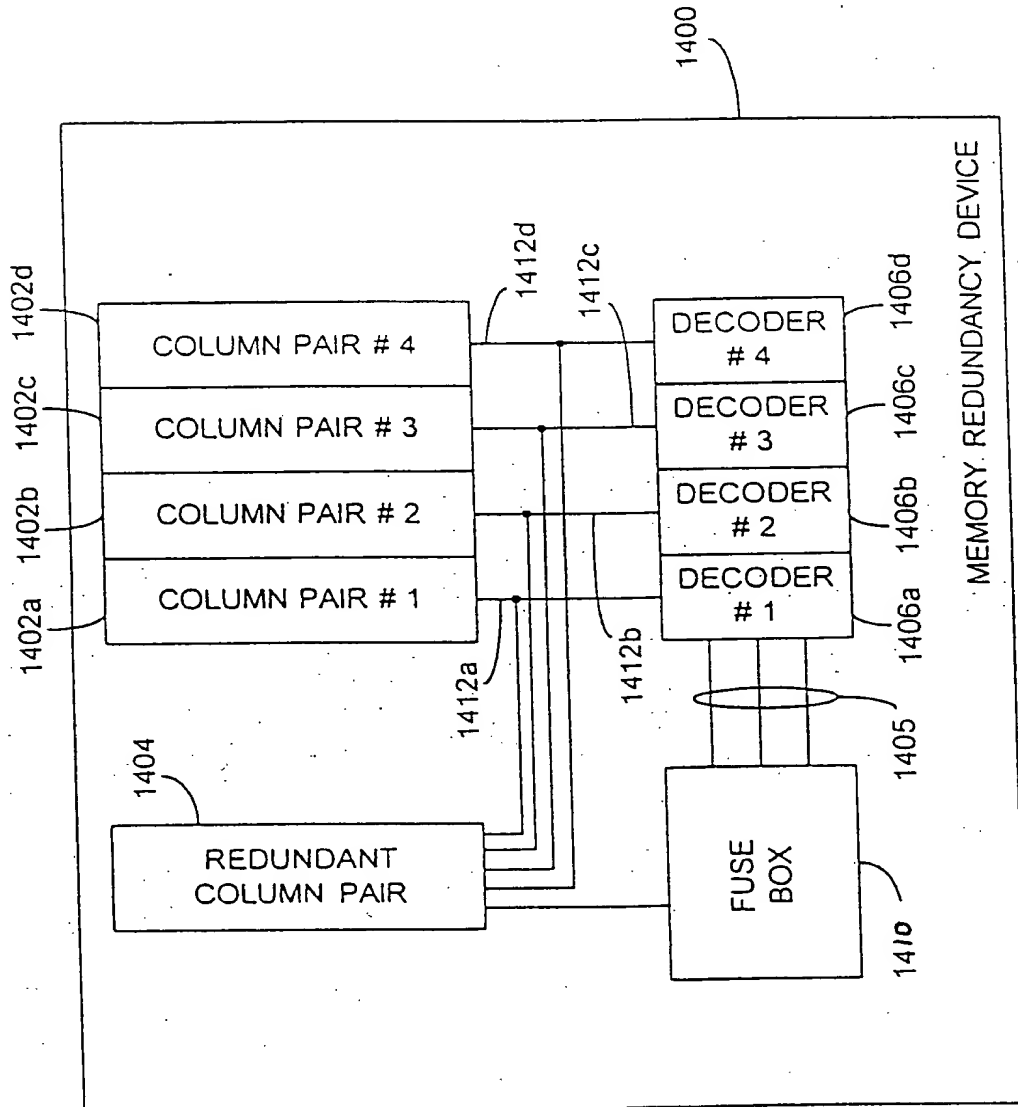
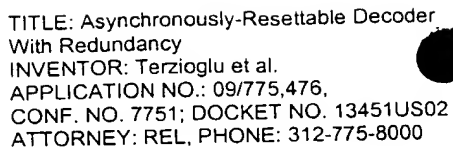
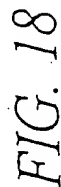


FIG. 14



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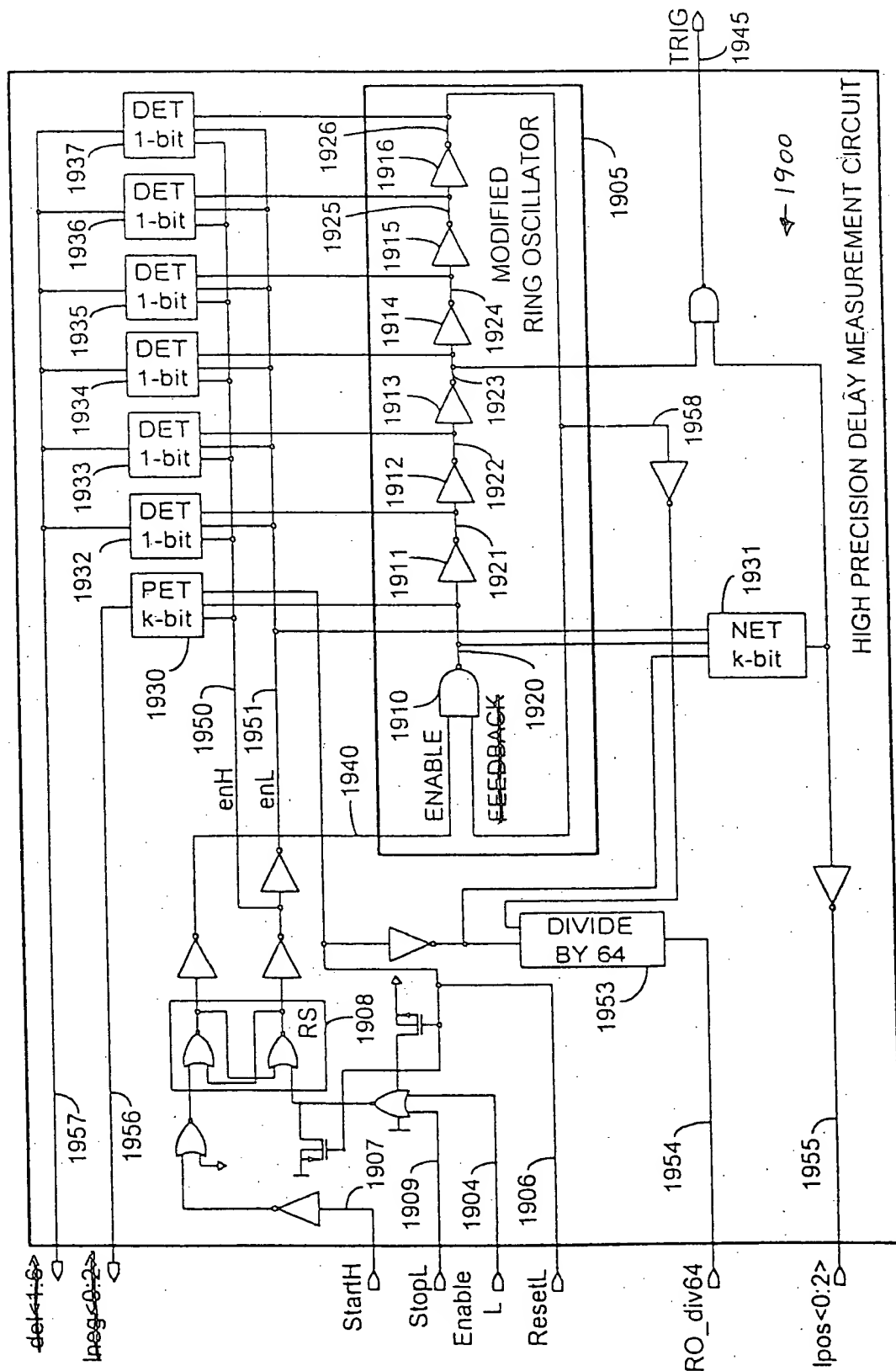


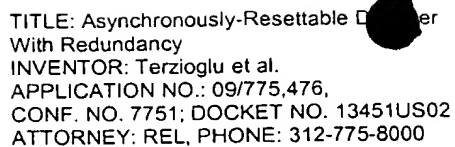


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